UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/826,039	04/16/2004	Hiroyasu Jobetto	04236/LH	9104

1933 7590 12/06/2005

FRISHAUF, HOLTZ, GOODMAN & CHICK, PC
767 THIRD AVENUE
25TH FLOOR
NEW YORK, NY 10017-2023

EXAMINER	
HA, NATHAN W	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 12/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/826,039	JOBETTO ET AL.	
	Examiner	Art Unit	
	Nathan W. Ha	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) *18-21 and 23-38* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17 and 22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of the species I, fig. 1, claims 1-17 and 22-23, in the reply filed on 10/11/05, is acknowledged. However, claim 23 does not belong to species I since the insulation layer in claim 23 is claimed to be made of organic material, while the insulation material in claim 1 is made of inorganic material as claimed in claim 3, which depends on claim 1. Therefore, species I includes only claims 1-17 and 22.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 3 and 13 recite the limitation "an insulating layer" in line 2. There is insufficient antecedent basis for this limitation in the claim. Since, it is unclear that these layer are the same as upper insulating layer as claimed in claim 1. Please check the entire claims for similar issue.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-2, 4, 6-9, 11, 13-17, and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Ma et al. (US 6,154,366, hereinafter, Ma.)

In regard to claims 1 and 22, in fig. 3k, Ma discloses a semiconductor device, comprising:

a semiconductor construction assembly having semiconductor substrate 106 which has one surface, the other surface 114 facing said one surface, and a plurality of side surfaces 116 between said one surface and the other surface, and has an integrated circuit element formed on the one surface, a plurality connection pads 108 which are arranged on said one surface and connected to the integrated circuit element, a protective layer 102 which is formed to cover the one surface of the semiconductor substrate and has openings for exposing the connection pads, and a plurality of conductors 124 which are connected the connection pads, arranged on the protective layer, and have pads;

an upper insulating layer which entirely covers 102' which entirely covers the one surface the semiconductor construction assembly including the conductors except the pads;

a sealing member 176 which covers at least side surface the semiconductor construction assembly; and

upper conductors 124' which are formed on the upper insulating layer, and has one ends electrically connected to the pads and an external connection pads 124",

respectively, an external connection pad of at least one of the upper conductors being disposed a region corresponding to the sealing member.

In regard to claim 2, Ma further discloses that the sealing member covers an entire periphery of the semiconductor construction assembly. See fig. 3k.

In regard to claim 4, wherein upper surfaces of the sealing member and the semiconductor construction assembly are flush with each other. See fig. 3k.

In regard to claim 6, wherein the semiconductor construction assembly has Columnar-shaped electrodes formed on the conductors. See fig. 3k.

In regard to claim 7, wherein the semiconductor construction assembly includes a sealing member, also 102', formed between the columnar- shaped electrodes.

In regard to claim 8, Ma further comprising a base member 172 which holds the semiconductor construction assembly and the sealing member. See fig. 3k.

In regard to claim 9 wherein the base member is made of heat dissipation material.

In regard to claims 11 and 13, and according to 112 rejection above, the office assumes that the insulating layer as mentioned in claim 13 is the same as the sealing member since there is no other insulating layer that is disclosed in the fig. 1, which is between the buried member and the chip. Hence, fig. 3k of Ma, in fact shows the sealing member includes a buried member as part of the sealing member, which is disposed horizontally on both sides of the chip. See fig. 2j, or 3k, and further shows the sealing member is between the chip and the buried layer.

In regard to claim 14, wherein interlayer conductors which connect the conductors of the semiconductor construction assembly and the upper conductors, and an interlayer dielectric layer which covers the interlayer conductors are arranged between the upper conductors and the semiconductor construction assembly. See fig. 2j.

In regard to claim 15, wherein an uppermost insulating layer is arranged on an upper surface of the dielectric layer including the upper conductors except the external connection pads of the upper conductors. See fig. 2j.

In regard to claim 16, wherein projecting connection terminals arranged on the external connection pads of the upper conductors. See fig. 2j.

In regard to claim 17, Ma further discloses that each of the projecting connection terminals includes a solder ball 156.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 3 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ma as applied to claims 1-2, 4, 6-9, 11, 13-17, and 22 above, and further in view of Chen et al. (US 2003/0133274, hereinafter, Chen.)

In regard to claim 3, Ma discloses all of the claimed limitations as mentioned above, except the material of the insulating layer is such inorganic material. Inorganic material is widely used to form insulation layers in semiconductor package in order to protect electrical circuits from physical damages or electrical damages such short circuit. For instance, Chen, in fig. 3G, for example, discloses an analogous semiconductor device including base element, semiconductor chip, and pads thereon. The pads are electrically protected and insulated by layer 320, which is made of inorganic material such as resin. See also paragraph [0024].

Therefore, it would have been obvious to one of ordinary skilled in the art at the time of the invention was made to use such material as taught by Chen in order to fully take the advantage as mentioned above.

In regard to claim 10, Chen further discloses that the semiconductor device is affixed to the substrate 310 by a non-conductive bonding material such as adhesive tape 410. See [0023].

8. Claims 5 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ma as applied to claims 1-2, 4, 6-9, 11, 13-17, and 22 above.

In regard to claims 5 and 12, Ma discloses all of the claimed limitations as mentioned above, except the thickness of the buried member and how the sealing member so that they are flush with each other.

At the time of the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the thickness of the above layers because applicant has not disclosed that these thicknesses provide an advantage, is used for a particular

purpose, or solve a stated problem. One of ordinary skill in the art, furthermore, would have expected applicant's invention to perform equally well with either shape because they perform the same function of insulating the devices.

Therefore, it would have been obvious to one of ordinary skill in the art to modify Main order to obtain the invention as specify in the above claims.

Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising therefrom. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nathan W. Ha whose telephone number is (571) 272-1707. The examiner can normally be reached on M-TH 8:00-7:00(EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nathan Ha
December 1, 2005